APPLICATION NOTE

PCA82C250 / 251
CAN Transceiver

AN96116

Philips
Semiconductors

PHILIPS

Abstract

The PCA82C250 and PCA82C251 are advanced transceiver products for use in automotive and general industrial applications with transfer rates up to 1 Mbit/s. They support the differential bus signal representation being described in the international standard for in-vehicle CAN high-speed applications (ISO 11898). Controller Area Network (CAN) is a serial bus protocol being primarily intended for transmission of control related data between a number of bus nodes.

This application note provides information how to use the above-mentioned transceiver products and discusses several topics of interest like slope control mode, stand-by mode, bus length and maximum number of bus nodes per network.

APPLICATION NOTE

PCA82C250 / 251 CAN Transceiver

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Summary

This report is intended to provide basic technical information for the implementation of the Physical Medium Attachment in a CAN network according to the ISO 11898 standard, using the transceiver products PCA82C250 and PCA82C251 from Philips Semiconductors. These products support bit rates up to 1 Mbit/s over a two-wire differential bus line, which is the transmission medium being specified by the ISO 11898 standard.

The report provides typical application circuit diagrams with and without electrical isolation and discusses several topics in more detail like slope control mode, stand-by mode, maximum bus length and maximum number of bus nodes per network.

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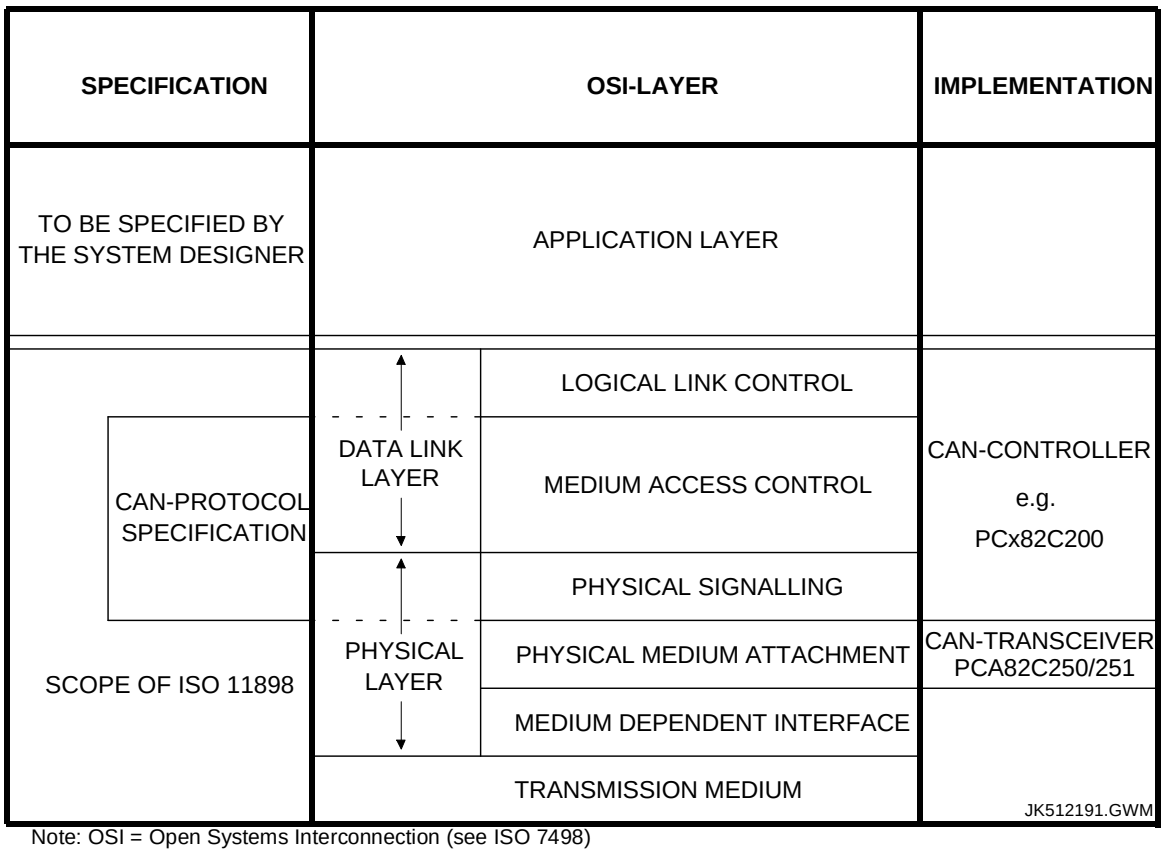
1. INTRODUCTION

ISO 11898 [3] is the international standard for in-vehicle high-speed communication using the Controller Area Network (CAN) bus protocol. The scope of this standard essentially is to specify the so-called data link layer and physical layer of the communication link. The physical layer is subdivided into three sublayers as shown in Fig. 1. These are

- Physical Signalling bit coding, timing and synchronization
- Physical Medium Attachment driver and receiver characteristics
- Medium Dependent Interface bus connector

This report focuses on the implementation of the Physical Medium Attachment sublayer using the transceivers PCA82C250 [1] and PCA82C251 [2] from Philips Semiconductors. The implementation of the Physical Signalling sublayer and the Data Link Layer is typically performed by integrated protocol controller products, like the PCx82C200 from Philips Semiconductors. Connection to the transmission medium is provided via the Medium Dependent Interface i.e. a connector used to attach bus nodes to the bus line.



Note: OSI = Open Systems Interconnection (see ISO 7498)

Fig. 1 Layered architecture of CAN

2. APPLICATION OF THE PCA82C250 AND PCA82C251

The PCA82C250/251 transceiver products basically provide interfacing between a protocol controller and a physical transmission line. They are designed to transmit data with a bit rate of up to 1 Mbit/s over a two-wire differential voltage bus line as described in the ISO 11898 standard. Their general features are listed in the data sheets (see [1] and [2]).

Both devices are designed for the use in CAN bus systems with a nominal supply voltage of 12 V (PCA82C250) and 24 V (PCA82C251) respectively. They are functionally identical and can be used in automotive and general industrial applications according to the relevant standards e.g. the ISO 11898 standard [3] and the DeviceNet™ Specification [5]. Both the PCA82C250 and the PCA82C251 can communicate to one another in one network. Moreover they are pin- & function-compatible i.e. they can be used with identical printed circuit boards.

Some main differences between both products are listed in Table 1.

Table 1 Main differences between PCA82C250 and PCA82C251

	PCA82C250	PCA82C251
Nominal system supply voltage	12 V	12V and/or 24 V
Maximum bus terminal DC voltage ($0 V < V_{CC} < 5.5 V$)	$-8 V < V_{CANL,H} < +18 V$	$-40 V < V_{CANL,H} < +40 V$
Maximum transient bus terminal voltage (ISO 7637)	$-150 V < V_{tr} < +100 V$	$-200 V < V_{tr} < +200 V$
Minimum transceiver supply voltage for extended fan out applications ($R_L = 45 \Omega$)	$V_{CC} > 4.9 V$	$V_{CC} > 4.5 V$

For general industrial applications the PCA82C251 is recommended to be employed as to e.g. its higher breakdown voltage and its capability to drive loads down to 45 Ω over the whole supply voltage range. Also the PCA82C251 draws less supply current in the recessive state and provides an enhanced bus output behaviour in power-fail situations.

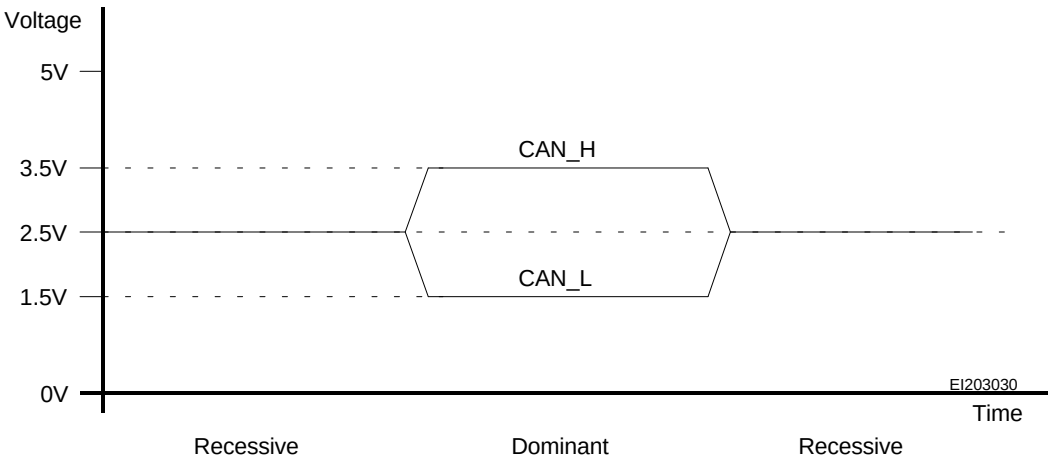
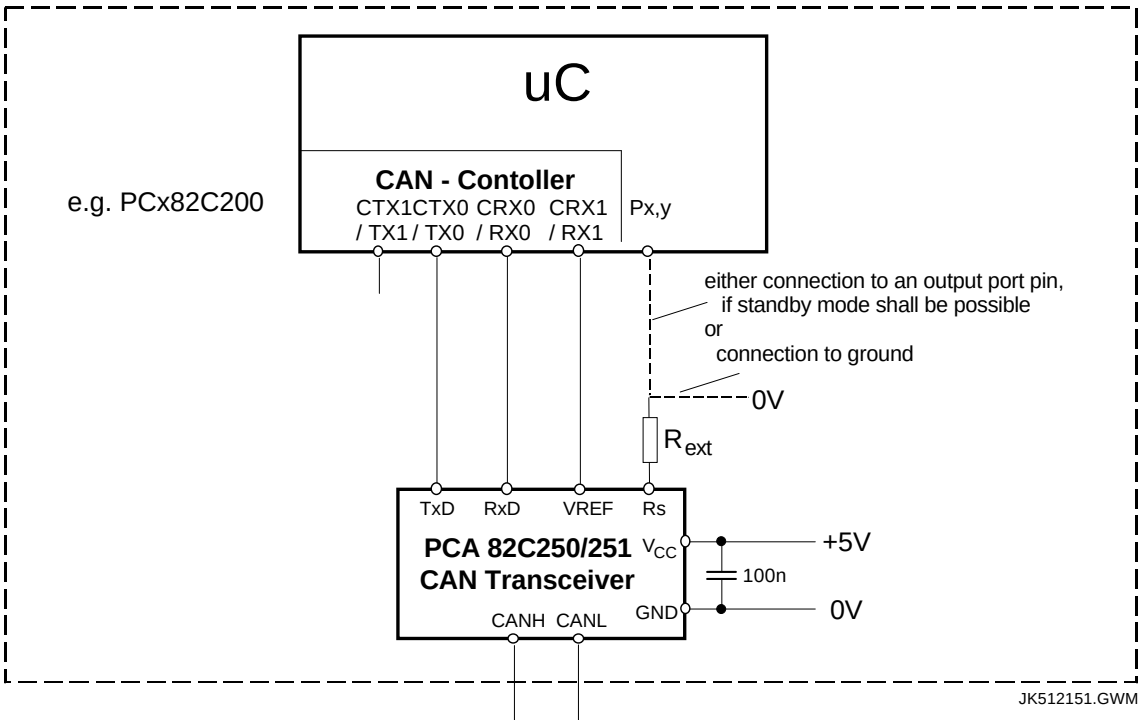


Fig. 2 Nominal bus levels according to ISO 11898



Programming of the Output Control Register (example)

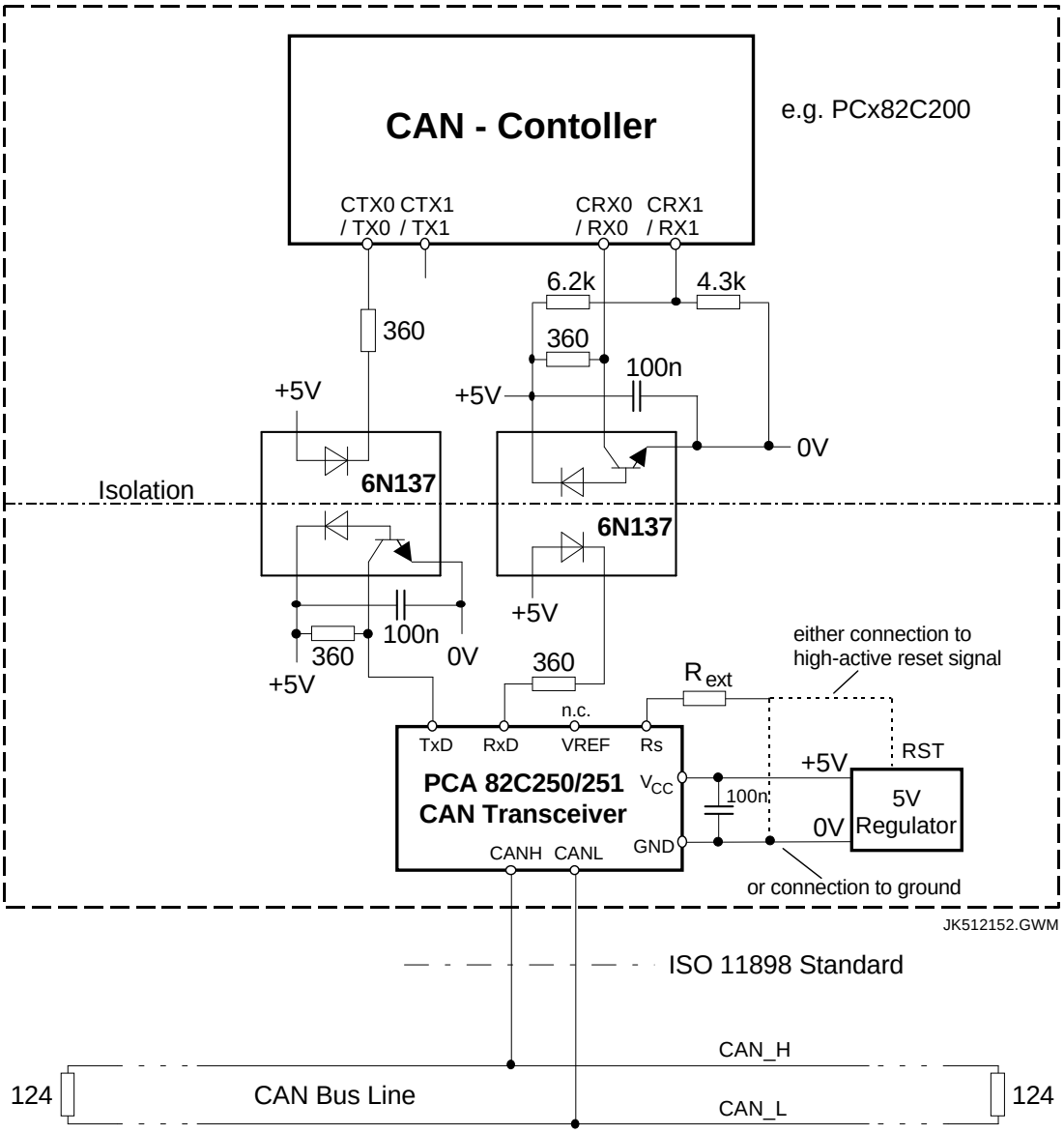
Output Control	TX0 push-pull, dominant = low	e.g. $1A_{hex}$

Fig. 3 Application example of the PCA82C250/251 transceivers

2.1 Application Examples

A typical application of the PCA82C250/251 transceiver is shown in Fig. 3. A protocol controller is connected to the transceiver via a serial data output line (TX) and a serial data input line (RX). The transceiver is attached to the bus line via its two bus terminals CANH and CANL, which provide differential receive and transmit capability. The input Rs is used for mode control purpose. The reference voltage output V_{REF} provides an output voltage of $0.5 \times V_{CC}$ nominal. Both transceiver products are powered with a nominal supply voltage of +5 V.

The protocol controller outputs a serial transmit data stream to the TxD input of the transceiver. An internal pull-up function sets the TxD input to logic HIGH i.e. the bus output driver is passive by default. In this so-called recessive state (see Fig. 2) the CANH and CANL inputs are biased to a voltage level of 2.5 V nominal via receiver input networks with an internal impedance of 17 kΩ typical. Otherwise if a logic LOW-level is applied to TxD, this activates the bus output stage, thus generating a so-called dominant signal level on the bus line (see Fig. 2). The output driver consists of a source and a sink output stage. CANH is attached to the source output and CANL to the sink output stage. The nominal voltage in the dominant state is 3.5 V for the CAN_H line and 1.5 V for the CAN_L line.



Programming of the Output Control Register (example)

Output Control	TX0 push-pull, dominant = low	e.g. $1A_{hex}$

Fig. 4 Application example for an interface with galvanic isolation using optocouplers

Note: If high bit rates shall be used, e.g. 500 kbit/s or above, then high-speed optocouplers should be considered with a delay of less than 40ns, e.g. HCPL-7101.

The bus line is in recessive state if no bus node transmits a dominant bit, i.e. all TxD inputs in the network are logic HIGH. Otherwise if one or multiple bus nodes transmit a dominant bit, i.e. at least one TxD input is logic LOW, then the bus line enters the dominant state thus overriding the recessive state (wired-AND characteristic).

The receiver comparator converts the differential bus signal to a logic level signal which is output at RxD. The serial receive data stream is provided to the bus protocol controller for decoding. The receiver comparator is always active i.e. it monitors the bus while the bus node is transmitting a message. This is required e.g. for safety reasons and to support the non-destructive bit by bit contention scheme of CAN. Some controller products provide an analog receive interface (RX0, RX1). In that case RX0 usually needs to be connected to the RxD output and RX1 needs to be biased to an appropriate voltage level. This can be done e.g. by using the V_{REF} output (see Fig. 3) or by using a resistive voltage divider (see Fig. 4).

In Fig. 3 the transceiver is directly connected to the protocol controller and its application circuitry. In cases where galvanic isolation is desired, optocouplers can be placed e.g. between the transceiver and the protocol controller as shown in Fig. 4. When using optocouplers one has to pay attention to choose the right default state when the circuitry at the protocol controller side of the isolation is not powered. In such a case the optocoupler being attached to TxD will be “dark” i.e. LED switched off. When this optocoupler is off/dark, then a logic HIGH-level has to be output to the TxD input of the transceiver for fail-safe purpose. Also if using optocouplers one may consider to attach the Rs mode control input to an active-high reset signal, e.g. to disable the transceiver when the local transceiver supply voltage is not OK e.g. during ramp-up and -down.

However using optocouplers generally increases the so-called loop delay of a bus node, if placed between the transceiver and the protocol controller. The signal has to pass these devices twice per node, i.e. transmit and receive path, which effectively decreases the maximum achievable bus length at a given bit rate. This fact has to be considered when calculating the maximum achievable bus length due to propagation delays in a CAN network. For more details please refer e.g. to [4].

2.2 Reference Voltage Output

The PCA82C250/251 provides a reference voltage output V_{REF}, which may be used e.g. to bias one of the inputs of a CAN protocol controller´s differential input comparator as shown in Fig. 3. In other cases a reference voltage may be generated locally at the protocol controller input as shown e.g. in Fig. 4. Which solution is appropriate in a system depends on the application and the bus input structure of the protocol controller product.

3. OPERATION MODES

The PCA82C250 and PCA82C251 provide three different operation modes. Mode control is being provided through the Rs control input.

The first mode is the high-speed mode supporting maximum bus speed and/or length.

The second mode is the so-called slope control mode which should be considered if unshielded bus wires shall be used. In this mode the output slew rate can be decreased intentionally, e.g. to reduce electromagnetic emission.

The third mode is the stand-by mode being of interest especially in battery powered applications, when the system power consumption needs to be very low. System reactivation is performed through transmission of a message. Fig. 3 gives an example for switching the transceiver between stand-by mode and normal operating mode.

- Px,y = HIGH: the PCA82C250/251 is switched to stand-by mode ($V_{Rs} > 0.75 \times V_{CC}$)
- Px,y = LOW: the PCA82C250/251 is switched to normal operating mode, which is either high-speed mode or slope control mode, depending essentially upon the resistance connected to Rs.

Usually the following resistance values for the slope-control resistor R_{ext} are suitable:

- $0\ \Omega < R_{ext} < 1.8\ k\Omega$ high-speed mode ($V_{Rs} < 0.3 \times V_{CC}$)
- $16.5\ k\Omega < R_{ext} < 140\ k\Omega$ slope control mode ($10\ \mu A < -I_{Rs} < 200\ \mu A$)

In the following these three operation modes shall be discussed in more detail.

3.1 High-Speed Mode

This mode is suitable to achieve a maximum bit rate and/or bus length. The high-speed mode is commonly employed in general industrial applications such as the CAN based system DeviceNet™. In this mode the bus output signals are switched as fast as possible and therefore a shielded bus cable usually would be appropriate to prevent a possible disturbance of e.g. a car radio by the bus signal.

The high-speed mode is selected with $V_{Rs} < 0.3 \times V_{CC}$. This can be achieved with a direct connection of the Rs control input to an output port of a microcontroller or ground potential or an active-high reset signal (see Fig. 3 and Fig. 4).

In high-speed mode the transceivers provide an effective loop delay of as low as 145 ns max. (155 ns for $T_{amb} > 85°C$). With view to the CAN bit timing requirements, the effective loop delay is the maximum of the dominant edge loop delay and the average value of dominant and recessive edge loop delay.

$$t_{loop.eff} = \max\{0.5 \times (t_{onRxD} + t_{offRxD}),\ t_{onRxD}\}$$

3.2 Slope Control Mode

In several applications the use of an unshielded bus cable will be desirable e.g. for system cost reasons. However using an unshielded cable implies additional requirements to be met by the transceiver product e.g. with view to electromagnetic compatibility (EMC). Using the PCA82C250/251 the slew rate of the bus signal can be decreased intentionally, which is recommended if an unshielded bus cable shall be used. The slew rate can be set via a series resistance value R_{ext} being connected to the control pin Rs. With respect to the CAN bit timing requirements a decreased slew rate implies an increase of the bus node loop delay and thus a lower bus length at a given bit rate or alternatively a lower bit rate at a given bus length. In slope control mode the bus output slew rate is basically proportional to the current flow out of pin Rs in the range of $10\ \mu A < -I_{Rs} < 200\ \mu A$ (see data sheets [1], [2]). If the Rs output current is in that range, then a voltage of approximately $0.5 \times V_{CC}$ will be output at the pin Rs. The transceiver is set to slope control mode when an appropriate resistance value is applied between the Rs pin and ground potential. As a rule of thumb the resistance value should be in the range of $16.5\ k\Omega < R_{ext} < 140\ k\Omega$ to meet the above-mentioned range for the Rs output current.

The suitable range for R_{ext} can be calculated using the limits for slope control mode

$10\ \mu A < -I_{Rs} < 200\ \mu A$ and $0.4 \times V_{CC} < V_{Rs} < 0.6 \times V_{CC}$.

The minimum and maximum values for R_{ext} can be calculated with the following two relations (for the explanation of the symbols see APPENDIX 1).

$$R_{ext} > \frac{0.6V_{CC.max}}{I_{Rs.max}} = \frac{0.6V_{CC.max}}{200\mu A} \quad (1)$$

$$R_{ext} < \frac{0.4V_{CC.min} - V_{OL.max}}{I_{Rs.min}} = \frac{0.4V_{CC.min} - V_{OL.max}}{10\mu A} \quad (2)$$

If the slope control resistor R_{ext} is connected to ground, then the value $V_{OL.max}$ is zero volts. The relation between the Rs output current and the bus signal slew rate is discussed in chapter 4.1.

3.3 Stand-by Mode

This mode is to be used when the power consumption needs to be minimized e.g. temporarily. The stand-by mode is selected with $V_{Rs} > 0.75 \times V_{CC}$.

Using the stand-by mode, the system power consumption can be reduced drastically. This mode is primarily intended for battery powered applications for example when a vehicle is parked. To enter stand-by mode a logic HIGH-level has to be applied to the transceiver´s control input Rs. This can be done either by direct connection of an output port pin to Rs or via any suitable slope control resistor R_{ext}. In stand-by mode the transmitter function and the receiver input bias network are switched off to reduce power consumption. The reference voltage output and a basic receive function will remain active and work with very low power consumption. This allows to reactivate the system via the bus line by transmission of a message. Upon detection of a dominant bus condition of at least 3 µs length, the transceiver will provide a wake-up interrupt signal to the protocol controller via its RxD output. Upon detection of a falling edge on RxD the controller should set the Rs pin to logic LOW-level in order to switch the transceiver back to normal transmission mode. As the receiver is slower in stand-by mode, it essentially depends on the delay time of the logic (falling edge on Rs) when the transceiver is back to normal reception speed. At high bus speeds the transceiver may not be able to correctly receive messages in stand-by mode i.e. while the Rs pin is still HIGH.

An alternative application is to connect the Rs input to an active-high reset signal. This can be done for example with view to the case of the transceiver and the protocol controller being supplied by different supply sources, e.g. if optocouplers are used (see Fig. 4).

4. SLOPE CONTROL FUNCTION

4.1 Slew Rate Calculation

As mentioned above, the slew rate (SR) of the bus output signal is proportional to the current flow (I_{Rs}) out of the pin Rs. As the current is primarily determined by the slope-control resistance value R_{ext}, a certain slew rate is achieved by applying a respective resistance. Note that there is a difference between the single-ended slew rate, which applies to each bus voltage individually and the differential signal slew rate, which applies to the differential voltage between CANH and CANL. Fig. 5 gives typical single-ended slew rate values as a function of the slope-control resistance value (see equation (4)).

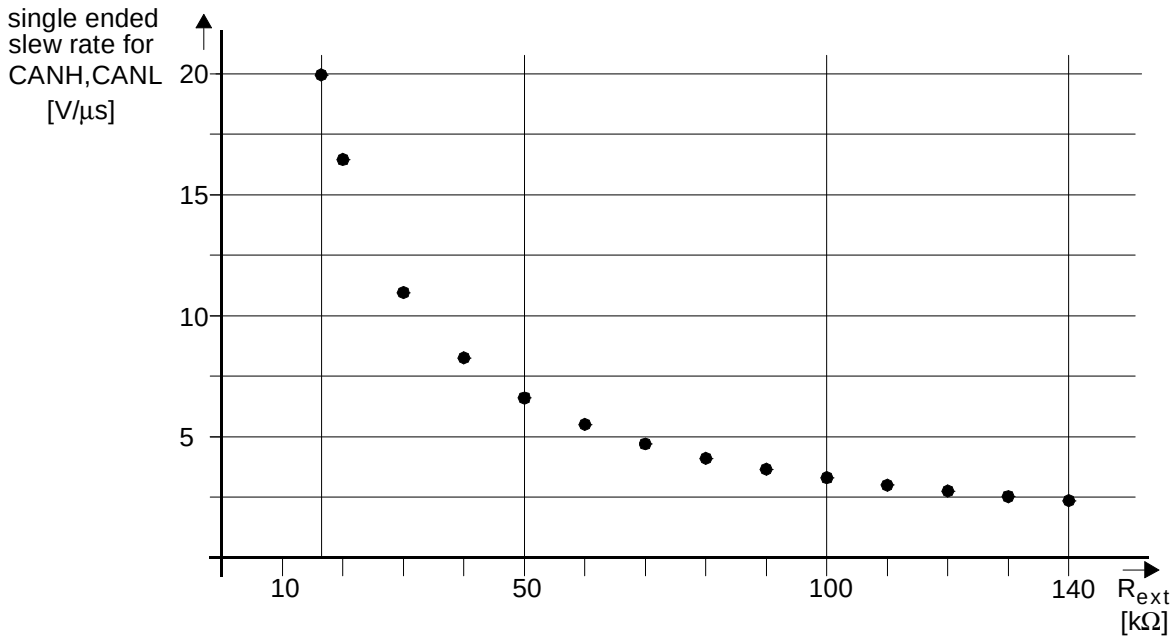


Fig. 5 Diagram: Slew rate versus slope control resistance value

These values are derived using the typical slew rate value given in the data sheets [1] and [2]:

SR (CANH or CANL) = 7 V/µs typ. at R_{ext} = 47 kΩ (connected between input Rs and 0 V, see Fig. 3)

In slope-control mode the Rs-voltage is $V_{Rs} = 0.5 \times V_{CC}$ typ.

As $I_{Rs} = \frac{V_{Rs}}{R_{ext}} = k_{SE} \times SR$ with k_{SE}: single-ended slew rate constant

the slew rate constant (single-ended) can be calculated using above typical values.

$$k_{SE} = \frac{0.5V_{CC}}{R_{ext} \times SR} = \frac{2.5V}{47k\Omega \times 7\frac{V}{\mu s}} = 7.6 \times 10^{-3}\frac{\mu s}{k\Omega} \quad (3)$$

Normally for slope control mode the resistor R_{ext} is connected between the input Rs and and a logic LOW-level (V_{OL}), provided either by a port output or a ground line. Thus the relation between the single-ended slew rate and the resistance R_{ext} is given by the following equation:

$$SR = \frac{V_{Rs} - V_{OL}}{k_{SE} \times R_{ext}} = \frac{V_{Rs} - V_{OL}}{7.6 \times 10^{-3} \frac{\mu s}{k\Omega} \times R_{ext}}. \quad (4)$$

Example 1:

With R_{ext} = 24 kΩ and V_{OL} = 0V the single-ended slew rate typically would be

$$SR = \frac{V_{Rs} - V_{OL}}{k_{SE} \times R_{ext}} = \frac{0.5 V_{CC}}{7.6 \times 10^{-3} \frac{\mu s}{k\Omega} \times R_{ext}} = \frac{0.5 \times 5V}{7.6 \times 10^{-3} \frac{\mu s}{k\Omega} \times 24 k\Omega} = 14 \frac{V}{\mu s}$$

Example 2:

To achieve a single-ended slew rate of 5 V/µs the typical slope-control resistance would be

$$R_{ext} = \frac{V_{Rs} - V_{OL}}{k_{SE} \times SR} = \frac{0.5 V_{CC}}{7.6 \times 10^{-3} \frac{\mu s}{k\Omega} \times SR} = \frac{0.5 \times 5\ V}{7.6 \times 10^{-3} \frac{\mu s}{k\Omega} \times 5 \frac{V}{\mu s}} = 66\ k\Omega \text{ ===> } R_{ext} = 68\ k\Omega$$

4.2 Bus Length in Slope Control Mode

In slope control mode the bus output slew rate is decreased intentionally, which implies an increase of the bus node loop delay. Due to the CAN bit timing requirements, this is equivalent to a reduction of the maximum bus line length at a given bit rate or reduction of the bit rate at a given bus length in a system compared to using the high-speed mode.

The maximum achievable bus line length is given by (see also [4]):

$$L_{max} = \frac{\frac{t_{prop}}{2} - t_{loop.eff} - t_{loop.eff.oth}}{t_p} \quad (5)$$

With L_{max} : Maximum achievable bus line length

t_{prop} : Maximum available two-way propagation delay (CAN bit timing)

$t_{loop.eff}$: Effective transceiver loop delay

$t_{loop.eff.oth}$: Effective loop delay of other components e.g. CAN controller and optocouplers

t_p : Specific bus line delay

From equation (5) it is obvious, that the maximum bus line length will increase, if the transceiver loop delay is decreased. The loop delay of a transceiver, which is set to the high-speed mode, is smaller than the loop delay of a transceiver, which is set to the slope control mode. Thus a higher bus line length can be achieved, if the transceiver is used in the high-speed mode, as a greater portion of the available propagation delay can be used for tolerating line delay.

This increase is given by the following equation:

$$\Delta L_{max} = \frac{t_{loop.eff}(\text{slope control mode}) - t_{loop.eff}(\text{high speed mode})}{t_p} = \frac{\Delta t_{loop.eff}}{t_p} \quad (6)$$

In a CAN network the effective maximum delay of a transceiver (also valid for the delay of other devices) are calculated using the following equation

(See APPENDIX 1 for an explanation of used symbols and abbreviations):

$$t_{loop.eff.max} = \max\{0.5 \times (t_{onRxD} + t_{offRxD}),\ t_{onRxD}\} \quad (7)$$

Table 2 gives an indication of the difference between using high-speed mode and slope control mode - in terms of maximum bus length. The values below refer to a specific propagation delay of t_p = 5 ns/m on the bus cable.

Table 2 Difference of maximum bus length

	Effective loop delay (upper limit at 125°C)			**Difference between both modes in terms of bus length**[1]
Product	slope-control mode[2]	high-speed mode	$\Delta t_{loop.eff}$	ΔL_{max}
PCA82C250	520 ns	155 ns	365 ns	~ 75 m
PCA82C251	550 ns	155 ns	395 ns	~ 80 m

1. At 5 ns/m specific propagation delay on the bus cable
2. Slope-control resistance R_{ext} = 47 kΩ

5. MAXIMUM BUS LINE LENGTH

The maximum achievable bus line length in a CAN bus network is determined essentially by the following physical effects:

1. The loop delays of the connected bus nodes (CAN controller, transceiver etc.) and the delay of the bus line
2. The differences in bit time quantum length due to the relative oscillator tolerance between nodes
3. The signal amplitude drop due to the series resistance of the bus cable and the input resistance of bus nodes

The effect 3. is discussed below.

The effects 1. and 2. are not discussed in this document (please refer e.g. to [4]). However as a rule of thumb the following bus line length can be achieved with the PCA82C250 and PCA82C251 in high-speed mode and with CAN bit timing parameters being optimized for maximum propagation delay:

Table 3 Bit Rate / Bus Length Relation

Bit Rate (kbit/s)	Bus Length (m)
1000	30
500	100
250	250
125	500
62.5	1000

5.1 Impact of the Bus Cable Resistance

The ISO 11898 Standard [3] assumes the network wiring topology to be close to a single line structure in order to minimize reflection effects on the bus line (Fig. 6).

At static conditions the differential input voltage at a bus node is determined by the current flowing through the differential input resistance of that node. In case of a dominant bit the output transistors of the transmitting node are switched on, causing a current flow, whereas the transistors are switched off for a recessive bit.

Thus the generated differential voltage at the input of a node ($V_{diff.in}$) depends on (see Fig. 7)

- The differential output voltage of the transmitting nodes ($V_{diff.out}$)
- The resistance of the bus cable ($R_W = \rho \times L$) with
  ρ = specific resistance per length unit and
  L = length of the bus line
- The differential input resistance of receiving nodes (R_{diff})

The worst case situation is given for one transmitting node at one end of the bus wire and a receiving node at the other end.

For this case the differential input voltage at the receiving node is calculated using Fig. 7 (see APPENDIX 2).

$$V_{diff.in} = \frac{V_{diff.out}}{1 + 2R_W \times \left(\frac{1}{R_T} + \frac{n-1}{R_{diff}}\right)} \quad (8)$$

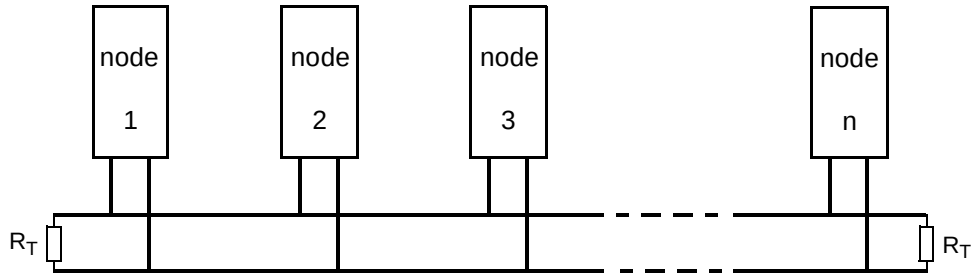


Fig. 6 Basic setup of a bus system (ISO 11898)

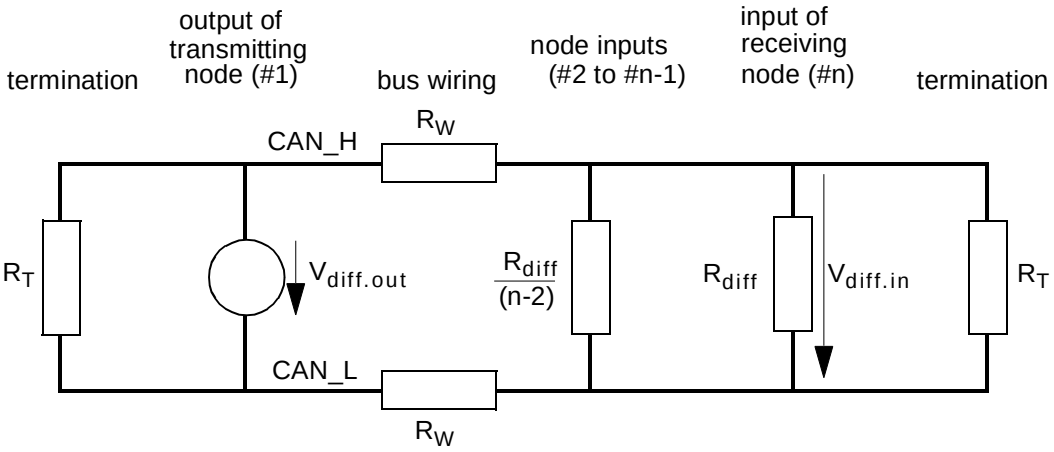


Fig. 7 Circuit diagram for the system setup of Fig. 6

A receiver recognizes a

recessive bit if the differential input voltage is below a level of 0.5V or 0.4V (see [1] and [2])

dominant bit if the differential input voltage is above a level of 0.9V or 1.0V (see [1] and [2])

The recessive level is generated by the bias network of the bus nodes and the termination resistors. The dominant level is determined by the drive capability of the transmitting node and the total network load resistance. Thus for proper detection of a dominant bit, a differential input voltage at the receiving node is requested ($V_{diff.in.req}$), which is given by the dominant threshold voltage of the receiver (V_{th}) and a user-defined safety margin. This safety margin can be considered as a fraction (k_{sm}) of the difference between the output level at the transmitting node and the receiver input threshold for detection of a dominant bit as shown in equation (9).

$$V_{diff.in.req} = V_{th} + k_{sm} \times (V_{diff.out} - V_{th}) \quad \text{with } k_{sm} = 0....1 \tag{9}$$

From equation (8) it is evident that the value of $V_{diff.in}$ for a dominant level is restricted by

- the minimum value of the differential output voltage for a dominant level ($V_{diff.out.min}$)
- the maximum value of the bus wire resistance ($R_{W.max}$)
- the minimum value of the termination resistors ($R_{T.min}$)
- the minimum differential input resistance of the nodes ($R_{diff.min}$)
- the maximum number of connected bus nodes (n_{max}).

This leads to the following relation

$$V_{diff.in.min} = \frac{V_{diff.out.min}}{1 + 2R_{W.max} \times \left(\frac{1}{R_{T.min}} + \frac{n_{max} - 1}{R_{diff.min}}\right)} \geq V_{diff.in.req} \qquad (10)$$

Equations (10) and (9) are the basis for calculating the maximum bus line length (see APPENDIX 3) dependent on

- the maximum number of nodes in a system (n_{max})
- the desired safety margin for detecting a dominant bit (k_{sm})
- the maximum specific resistance per length unit (cross section) of the used cable (ρ_{max}).

$$L_{max} \leq \frac{1}{2 \times \rho_{max}} \times \left(\frac{V_{diff.out.min}}{V_{th.max} + k_{sm} \times (V_{diff.out.min} - V_{th.max})} - 1\right) \times \frac{R_{T.min} \times R_{diff.min}}{R_{diff.min} + (n_{max} - 1) \times R_{T.min}} \qquad (11)$$

Using this equation the maximum bus line length for different wire types and a different number of connected nodes can be calculated. Some examples are given in Table 6.

5.2 Maximum Number of Nodes

The transceivers PCA82C250 and PCA82C251 provide an output drive capability down to a minimum load of $R_{L.min}$ = 45 Ω. If the PCA82C250 is used, a supply voltage of V_{CC} > 4.9 V is needed for driving a load of R_L = 45Ω (see Table 1). The number of nodes which can be connected to a network depends e.g. on the minimum load resistance a transceiver is able to drive. This maximum number of nodes can be calculated using the circuit diagram of Fig. 7. For worst case consideration the bus line resistance R_W is considered to be zero.

This leads to the following relations for calculating the maximum number of nodes:

$$\frac{R_{T.min} \times R_{diff.min}}{(n_{max} - 1) \times R_{T.min} + 2R_{diff.min}} > R_{L.min} \quad ===> \quad n_{max} < 1 + R_{diff.min} \times \left(\frac{1}{R_{L.min}} - \frac{2}{R_{T.min}}\right)$$

As the minimum differential input resistance of the PCA82C250/251 transceivers is $R_{diff.min}$ = 20 kΩ, the following maximum number of bus nodes can be connected:

106 nodes for R_T = 118 Ω and R_L = 45 Ω ; (V_{CC} > 4.9V if 82C250 is used)

112 nodes for R_T = 120 Ω and R_L = 45 Ω ; (V_{CC} > 4.9V if 82C250 is used)

5.3 Examples

Table 4 provides a first indication on which kind of wire cross section should be considered for the signal pair of the bus trunk cable.

Table 4 Minimum recommended bus wire cross-section for the trunk cable[1]

Bus Length / Number of Nodes	32	64	100
100 m	0.25 mm^2 or AWG 24	0.25 mm^2 or AWG 24	0.25 mm^2 or AWG 24
250 m	0.34 mm^2 or AWG 22	0.5 mm^2 or AWG 20	0.5 mm^2 or AWG 20
500 m	0.75 mm^2 or AWG 18	0.75 mm^2 or AWG 18	1.0 mm^2 or AWG 18

1. Assumptions for Table 4: 32 nodes : $R_w < 21\ \Omega$
64 nodes : $R_w < 18.5\ \Omega$
100 nodes: $R_w < 16\ \Omega$

For the drop cables a wire cross section of 0.25 to 0.34 mm^2 (or AWG 24, AWG 22) would be an appropriate choice in many cases.

Based on the discussion in chapter 5.1 and chapter 5.2, the following examples list the maximum achievable bus line length, calculated for bus cables being specified in the ISO 11898 standard [3] and in the Device Net™ specification [5]. The specific cable resistance for the cables used are given in Table 5.

Table 5 Specific resistance of different cables (1 km = 3280.84 ft., 1 ft. = 0.3048 m)

Cable type	Specific cable resistance	
	ρ_{nom} [Ω/km]	ρ_{max} [Ω/km]
ISO 11898 (automotive): 0.25 mm^2 (or AWG23)	70	90 [1]
Device Net™ thin cable	69	92
Device Net™ thick cable	18	23
0.5 mm^2 (or AWG20)	37	50 [1]
0.75 mm^2 (or AWG18)	26	33 [1]

1. Assumed value

With the known values for

the minimum dominant value	: $V_{diff.out.min}$	= 1.5 V	see [1] and [2]
the minimum differential input resistance	: $R_{diff.min}$	= 20 kΩ	see [1] and [2]
the requested differential input voltage	: $V_{th.max}$	= 0.9V or 1.0 V	see [1] and [2]
the minimum termination resistance of	: $R_{T.min}$	= 118 Ω	see [3]

the maximum wiring length is calculated for different bus cable types and a different number of connected bus nodes using equation (11) on page 19. The result is listed in Table 6.

Table 6 Maximum bus cable length for different cables and number of nodes (n)

Cable Type	L_{max} (k_{sm} = 0,2)[1]			L_{max} (k_{sm} = 0,1)[2]		
	n = 32	n = 64	n = 100	n = 32	n = 64	n = 100
DeviceNet™ (thin cable) and/or ISO 11898 cable	200 m	170 m	150 m	230 m	200 m	170 m
DeviceNet™ (thick cable)	800 m	690 m	600 m	940 m	810 m	700 m
0.5 mm^2 (or AWG 20)	360 m	310 m	270 m	420 m	360 m	320 m
0.75 mm^2 (or AWG 18)	550 m	470 m	410 m	640 m	550 m	480 m

1. Calculated with $V_{th.max}$ = 1.0 V and a safety margin of k_{sm} = 0.2
2. Calculated with $V_{th.max}$ = 1.0 V and a safety margin of k_{sm} = 0.1

Note: If driving more than 64 bus nodes and/or more than 250 m bus length the accuracy of the V_{CC} supply voltage for the PCA82C251 is recommended to be 5% or better. The PCA82C250 needs a supply voltage of at least 4.75V when driving 50 Ω load, i.e. 64 bus nodes, and at least 4.9V when driving 45 Ω load, i.e. 100 bus nodes.

6. BUS TERMINATION AND TOPOLOGY ASPECTS

Generally the CAN high-speed standard ISO 11898 provides a single line structure as network topology. The bus line is terminated at both ends with a single termination resistor. However in practice some deviation from that topology may be needed to accommodate appropriate drop cable length of e.g. a few meters. Also a modified termination network may be desirable in some applications e.g. for EMC related considerations. In this chapter some modified bus termination concepts as well as topology aspects shall be discussed.

6.1 Split Termination Concept

This is an option intended to provide enhanced EMC characteristics without changing the DC characteristics of the terminated line. Basically each of the termination resistors is split into two resistors of equal value, i.e. two resistors of 62 Ω instead of one resistor of 124 Ω (see Fig. 8). The special characteristic of this approach is, that the so-called common-mode signal is available at the centre tap of the termination. As the common-mode signal is simply a DC voltage in the ideal case, this centre tap can be grounded via a capacitor of e.g. 10 nF to 100 nF. However it is obvious, that the capacitor should be connected to a “quiet” ground level. For example a separate ground lead to the connector´s ground pin is recommended, if termination is placed inside of bus nodes.

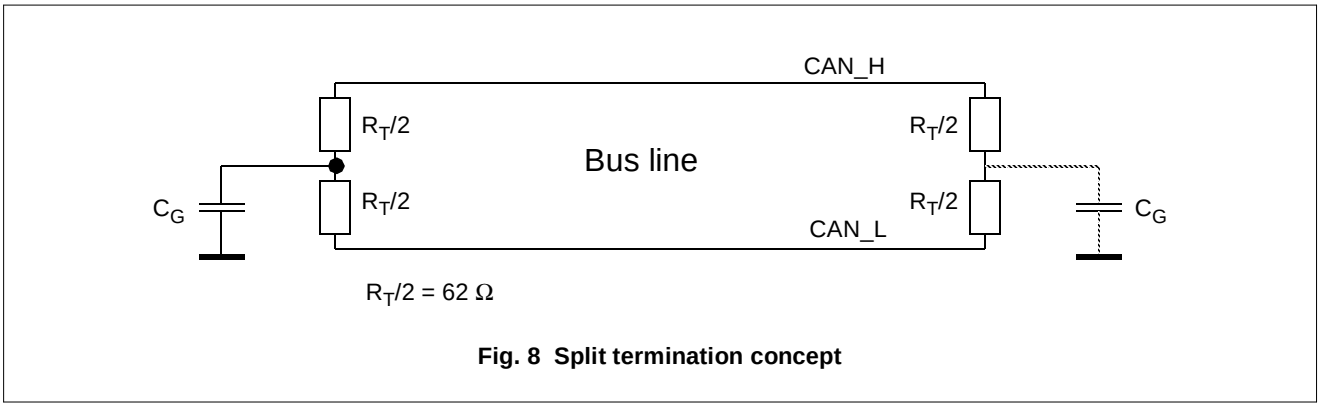


Fig. 8 Split termination concept

Basically there are two options with different advantages and disadvantages. The first option includes both termination resistors to be split and grounded. This is the preferred approach to optimize the characteristic in the higher frequency range. However there is a chance that there are unwanted loop currents via ground potential, as both termination resistors are grounded. In that case one may consider to ground only one of the termination resistors. This can provide a better characteristic in the medium to low frequency range. As mentioned above, the DC characteristics of the terminated bus line is not changed.

6.2 Multiple Termination Concept

This concept can be used in combination with the split termination concept above and targets at network topologies which differ from a single line structure.

In some applications a topology different from a single line structure is needed, e.g. a star topology with three branches (see Fig. 9). To accommodate such a topology, the multiple termination concept may be considered. Essentially this approach suggests, that the total termination resistance, i.e. 62 Ω, is being distributed over more than two resistors. If for example a star topology is needed with three branches, then one may consider to terminate each branch with about three times the total termination resistance, i.e. 180 Ω. With this approach it is essential that the total termination resistance (i.e. all termination resistors in parallel) does suit the transceiver´s output drive capability. If one of the branches is optional, e.g. for temporary attachment of diagnostic equipment, then the trunk line would be terminated via two resistors of 180 Ω and the optional branch would be terminated via another termination resistor of 180 Ω. It is obvious that this concept implies some mismatch between charac-

teristic line impedance and termination resistance. However this is not considered to be critical, provided there is a sufficient safety margin left with view to the CAN bit timing parameters.

As a rule of thumb the total bus length including all branches shall be less than the suitable bus length for the single line structure in a given configuration. For example instead of a single line structure of 100 m length a 3-branch star topology may be considered with each branch being terminated with 180 Ω and a drop length of less than 33 m each. The basic network is recommended to be terminated with at least 50% of the nominal termination resistance i.e. when all optional parts are disconnected, the remaining “basic” termination resistance is recommended to be less than 120 Ω (e.g. 2 x 180 Ω or 3 x 240 Ω, etc.).

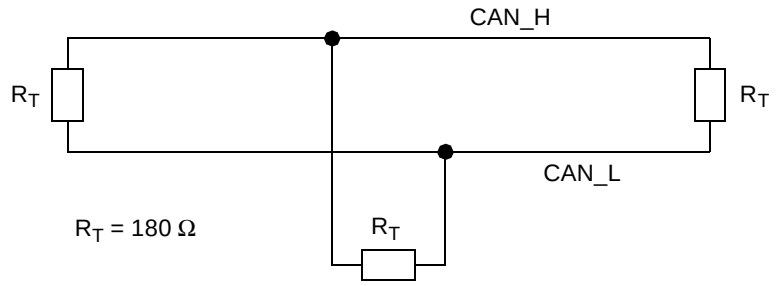


Fig. 9 Multiple termination concept (example)

6.3 Single Termination Concept

In some cases only a single termination resistor, e.g. 124 Ω or 62 Ω, is desired inside e.g. a master node. This is suitable when the system configuration provides a considerable safety margin with view to the CAN bit timing requirements. As a rule of thumb the total line length should be less than 50% of the length with the normal termination concept.

6.4 Termination Mismatch

This concept supposes an intentional mismatch between the termination resistance and the characteristic line impedance, e.g. to decrease the required wire cross section, to increase fan-out or to reduce power consumption in a given configuration.

Essentially this approach implies termination resistance values being higher than the characteristic cable impedance. Termination mismatch can be suitable when the system configuration provides a large safety margin with view to the CAN bit timing requirements, i.e. the bit rate or bus length is considerably reduced compared to the limit with the standard termination concept. This is needed due to the fact, that the bus line related delay will significantly increase when the termination resistance is increased. In any case the differential termination resistance is recommended to be less than 500 Ω, i.e. 2 x 1 kΩ should be considered as an upper limit independent of the bit rate used. Note, that the value for the two-way bus line propagation delay is related to the bus time constant, i.e. the capacitance of the entire network times the effective discharge resistance (e.g. 60 Ω). Also one needs to consider, that ground offset between the bus nodes increases the time needed to discharge the network capacitance.

6.5 Unterminated Cable Drop Length

Initially the topology of a CAN bus system is considered to be close to a single line structure. However in a number of cases some deviation from this topology may be needed, e.g. for temporary attachment of diagnostic equipment to the bus line. Also bus nodes will often be connected to the bus line via an unterminated drop cable.

When unterminated drop cables are connected, some reflection effects will occur on the bus line. Reflection is not necessarily a problem, as the network will provide some robustness thanks to e.g. receiver hysteresis and the synchronization rules of the CAN protocol. Reflected waves are assumed to disappear once they arrive at one of the bus line ends being terminated with the characteristic cable impedance. Essentially it depends on the bit timing parameters, the trunk cable length and the drop cable length whether reflections will be tolerated.

Basically it is advisable to specify an upper limit for the drop length and an upper limit for the so-called cumulative drop length. The cumulative drop length is the sum of all drop cable length. As a rule of thumb, the following relation can be considered for the cable drop length:

$$L_u < \frac{t_{PROPSEG}}{50 \times t_p} \tag{12}$$

With $t_{PROPSEG}$ being the length of the propagation segment of the bit period i.e. the length of time segment 1 (TSEG1) minus the length of the resynchronization jump width (SJW), t_p being the specific line delay per length unit (e.g. 5 ns/m) and L_u representing the length of the unterminated cable stub.

As to the cumulative drop length the following relation can be considered as a rule of thumb:

$$\sum_{i=1}^{n} L_{ui} < \frac{t_{PROPSEG}}{10 \times t_p} \tag{13}$$

In addition to that, the actual propagation delay on the bus line should be calculated on the basis of the total line length i.e. trunk cable plus all drop cable length. This effectively leads to a reduction of the maximum trunk cable length by the sum of the actual cumulative drop cable length at a given bit rate. If the above recommendations are met, then the probability of reflection problems is considered to be fairly low.

Example:

Bit Rate = 500 kbit/s , $t_{PROPSEG} = 12 \times 125$ ns = 1500 ns , t_p = 5 ns/m

$$L_u < \frac{t_{PROPSEG}}{50 \times t_p} = \frac{1500\text{ns}}{50 \times 5\ \frac{\text{ns}}{\text{m}}} = 6\ \text{m}$$

$$\sum_{i=1}^{n} L_{ui} < \frac{t_{PROPSEG}}{10 \times t_p} = \frac{1500\text{ns}}{10 \times 5\ \frac{\text{ns}}{\text{m}}} = 30\ \text{m}$$

As a rule of thumb an unterminated drop cable should be shorter than 6 m and the cumulative drop length should be less than 30 m for a CAN propagation segment (PROP_SEG) length of 1500 ns.

7. CONCLUSION

The PCA82C250 and PCA82C251 are advanced transceiver products being suitable for usage in automotive as well as general industrial applications with bit rates up to 1 Mbit/s. They support a differential bus signal representation as described in the international standard for in-vehicle high-speed applications (ISO 11898) using the Controller Area Network (CAN) protocol.

Enhanced electromagnetic compatibility (EMC) performance is provided through an extended common-mode range of -7V to +12V and the slope-control function, where the slew rate of the bus signal can be adjusted via a resistance value. For battery powered applications a stand-by mode is provided to drastically reduce power consumption of the network, e.g. when a vehicle is parked. In stand-by mode the network is being activated via the bus lines upon detection of a message.

The PCA82C250 and PCA82C251 are proof against short-circuit conditions on the bus outputs and usual transients in an automotive environment (ISO 7637). Moreover a thermal shutdown function protects the devices against thermal overload e.g. due to short-circuit conditions. Both products are designed for connection to the protocol controller or bus line with a minimum number of external components.

Also both products are capable of driving a large number of bus nodes i.e. 64 to 100 per network, and bus length of up to about 0.5 to 1 km, which is advantageous primarily in general industrial applications such as the CAN based system DeviceNet^{TM}.

The PCA82C250 and PCA82C251 are pin- and function compatible and operate in a wide supply voltage range of 5 V $\pm$ 10%. For general industrial applications the PCA82C251 should be used because of e.g. its larger drive capability and higher breakdown voltage protection at the bus outputs.

The advanced functionality being described above makes the PCA82C250 and PCA82C251 an attractive choice in many automotive and general industrial applications.

8. LIST OF REFERENCES

[1] Data Sheet PCA82C250, Philips Semiconductors, September 1994

[2] Data Sheet PCA82C251, Philips Semiconductors, October 1995

[3] Road vehicles - Interchange of digital information - Controller area network (CAN) for high-speed communication, ISO 11898, International Standardization Organization, 1993

[4] CAN Bit Timing, Application Note, Philips Semiconductors, 1996 (to be published)

[5] DeviceNet Specification, Volume I, Release 1.3, Open DeviceNet Vendor Association Inc., December 1995

APPENDIX 1 ABBREVIATIONS AND DEFINITIONS

SR		single-ended slew rate of the signal transition at CANL and/or CANH
k_{SE}		single-ended slew rate constant (in slope control mode the slew rate is proportional to the current out of pin Rs of the transceiver)
I_{Rs},	$I_{Rs.min}$, $I_{Rs.max}$	current (minimum, maximum) at pin Rs of the transceiver
V_{Rs}		typical voltage at pin Rs of the transceiver
$P_{x,y}$		digital output port pin of a controller IC for transceiver mode control
V_{OL},	$V_{OL.max}$	nominal (maximum) LOW-level output voltage of the controller output port
R_{ext},	$R_{ext.min}$, $R_{ext.max}$	nominal (minimum, maximum) value of the slope-control resistor at pin Rs of the transceiver. This value determines the current and thus the slew rate at CANL and CANH
V_{CC},	$V_{CC.min}$, $V_{CC.max}$	nominal (minimum, maximum) value of the transceiver supply voltage
$t_{loop.eff}$,	$t_{loop.eff.oth}$	effective transceiver (other components) loop delay
$\Delta t_{loop.eff}$		difference between the effective loop delay of the transceiver in slope control mode and in high-speed mode
t_{prop}		available two-way propagation delay (limited by CAN bit timing parameters)
t_p		specific line delay per length unit (e.g. 5 ns/m)
t_{onRxD},	t_{offRxD}	loop delay of the transceiver between pin TxD (transmit data input) and RxD (receive data output) at switching from recessive to dominant (dominant to recessive) state (see [1] and [2])
$t_{PROPSEG}$		length of the propagation segment of the bit period i.e. length of segment 1 (TSEG1) minus length of the resynchronization jump width (SJW)
$V_{diff.in}$,	$V_{diff.in.min}$, $V_{diff.in.req}$	nominal (minimum, requested) differential input voltage for reception
$V_{diff.out}$,	$V_{diff.out.min}$	nominal (minimum) differential output voltage at the transmitting node
V_{th},	$V_{th.max}$	nominal (maximum) differential input threshold voltage for detection of a dominant bus condition
k_{sm}		a factor indicating the safety margin for the differential input voltage for detecting a dominant bit at reception ($0 < k_{sm} < 1$)
R_{diff},	$R_{diff.min}$	nominal (minimum) differential input resistance of a bus node in recessive state (TxD = HIGH)
n,	n_{max}	number (maximum number) of bus nodes in the network
R_T,	$R_{T.min}$	nominal (minimum) value for the bus termination resistors
R_W,	$R_{W.max}$	nominal (maximum) series resistance of the bus wires
L,	L_{max}	length (maximum length) of the bus wires between any two bus nodes
L_u		length of the unterminated cable stub.
ρ,	ρ_{typ}, ρ_{max}	specific (typical, maximum) resistance per length unit of the bus wires
R_L,	$R_{L.min}$	total (minimum total) differential resistive bus load as seen by the transmitting node

APPENDIX 2 CALCULATION OF THE VOLTAGE AT THE INPUT OF A NODE

For the calculation of the worst case (i.e. minimum) differential input voltage at the receiving node the following assumptions or simplifications are made (see also Fig. 7 and Fig. 10):

- The termination resistors (R_T) are located at the output of the transmitting and at the input of the receiving node.
- The resistance of the lines between the transmitting and the receiving node is represented by the resistors R_W.
- All other nodes are at the same end of the transmission line as the receiving node resulting in the minimum differential input voltage.
- The output voltage of the transmitting node ($V_{diff.out}$) is supposed to be generated by a voltage source.

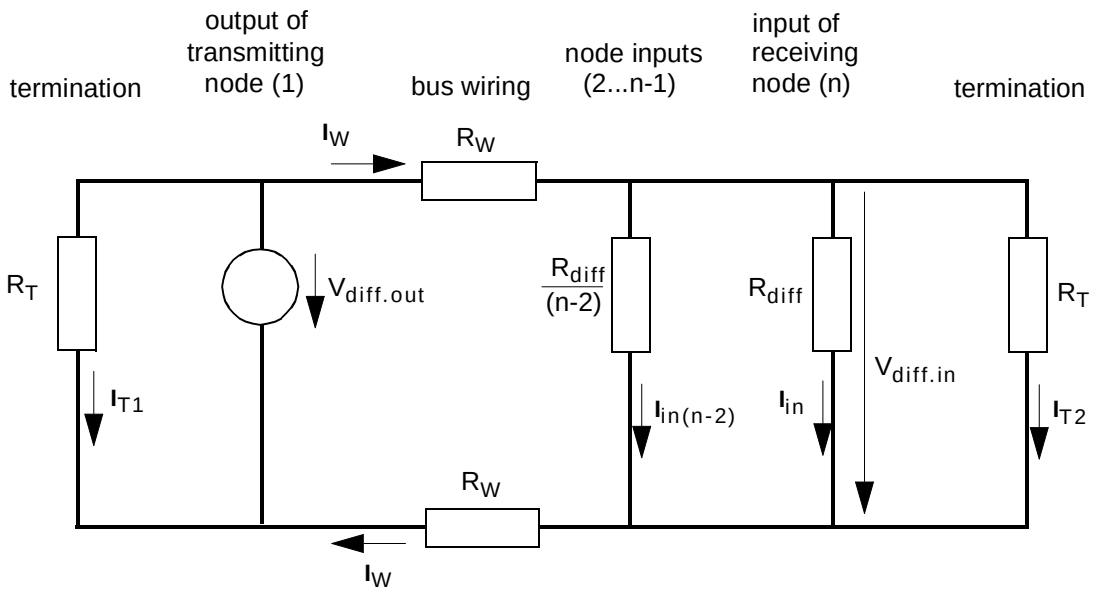


Fig. 10 Circuit diagram used for the calculation of the differential input voltage at the receiver node.

Thus the relation between the achievable differential input voltage at the receiving node and the differential output voltage of the transmitting node is given by:

$$V_{diff.out} = V_{diff.in} + 2 \times R_W \times I_W \quad (14)$$

The current I_W flowing through the bus lines splits up in $I_{in(n-2)}$ (input current of the connected nodes without the transmitting and receiving one), I_{T2} (current flowing through the termination resistor) and I_{in} (input current of the receiving node) as shown in Fig. 10.

With $I_W = I_{in(n-2)} + I_{T2} + I_{in}$ and

$$V_{diff.in} = I_{in(n-2)} \times \frac{R_{diff}}{n-2} \quad \text{and} \quad V_{diff.in} = I_{T2} \times R_T \quad \text{and} \quad V_{diff.in} = I_{in} \times R_{diff}$$

the relation between $V_{diff.out}$ and $V_{diff.in}$ is calculated from equation (14)

$$V_{diff.out} = V_{diff.in} + 2 \times R_W \times V_{diff.in} \times \left(\frac{1}{R_T} + \frac{n-1}{R_{diff}} \right) \quad (15)$$

Equation (8) on page 17 is derived from equation (15).

APPENDIX 3 CALCULATION OF THE MAXIMUM BUS LINE LENGTH

Under worst case conditions the minimum differential input voltage of a dominant level at the receiving node must be higher than the sum of the worst case switching threshold of the input transistor and a certain safety margin, which is requested in the system. The requested input voltage was given by equation (9) on page 18. The worst case value is given by

$$V_{diff.in.req} = V_{th.max} + k_{sm} \times (V_{diff.out.min} - V_{th.max}) \qquad \text{with} \quad k_{sm} = 0....1 .$$

Thus the relation (10) on page 19 is changed to

$$V_{diff.in.min} = \frac{V_{diff.out.min}}{1 + 2R_{W.max} \times \left(\frac{1}{R_{T.min}} + \frac{n_{max}-1}{R_{diff.min}} \right)} \geq V_{th.max} + k_{sm} \times (V_{diff.out.min} - V_{th.max}) \quad . \quad (16)$$

With the definition

$$R_{W.max} = \rho_{max} \times L_{max}$$

the maximum wiring length is determined using equation (16):

$$L_{max} \leq \frac{1}{2 \times \rho_{max}} \times \left(\frac{V_{diff.out.min}}{V_{th.max} + k_{sm} \times (V_{diff.out.min} - V_{th.max})} - 1 \right) \times \frac{R_{T.min} \times R_{diff.min}}{R_{diff.min} + (n_{max} - 1) R_{T.min}}$$